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09/532,611	03/22/2000	Paul M. Elliot	1314.3002R1	8811

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IP STRATEGIES, PC
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EXAMINER	
LEE, TIMOTHY L	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/532,611	ELLIOTT ET AL.	
	Examiner	Art Unit	
	Timothy Lee	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 3, 4, 7, 8, 9-11, 13, 15-17, 18, 22 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,188,686) in view of Laor et al. (US 6,424,649).

3. Regarding claims 1 and 35, Smith discloses a switching apparatus that includes a plurality of input ports and a plurality of output ports. See Figs. 2 and 13. Smith discloses that ATM cells are received at the data ports DP0 to DP127 from AMT channels connected to these ports. The ATM channels may be CBR, VBR, ABR, or others (from first interface card to second interface card...capable of supporting multiple types of interfacing cards; a plurality of interface cards for transmitting and receiving data streams). See col. 13, line 51-col. 14, line 6. The system contains a switching controller 20 that is connected to all of the data units and all the connection units and also the switching units (a control unit for controlling the operation of the apparatus). See col. 13, lines 39-47. Fig. 6 shows that the switching units contain a set of multiplexers, where each multiplexer can receive data from multiple lines and output them onto one line (...combining the received data streams so as to generate at least one cross-connected data stream...transmitting the data stream to the interface cards). See Figs. 6 and 6, and col. 18, line 29-col. 19, line 32. As can be seen in Figs. 2 and 13, the ports (interface cards) can be connected to each other through the switching units (parallel data buses, for providing

connectivity between each of said plurality of interface cards). Smith does not expressly disclose a clock recovered bus without synchronization information. Laor et al. discloses a switch that operates asynchronously, but appears to operate synchronously by using a single clock signal source which is uniform for the switch interconnect and its input and output queues. See col. 1, lines 38-47. The input interfaces include a PLL which synchronizes to the single frequency source once for all serial communication to the switch interconnect. The PLL's are used for synchronization purposes so that synchronization information doesn't have to be sent in the packets. See col. 1, lines 61-67. It would have been obvious to use the asynchronous switch with PLL's in the system disclosed by Smith. One would have been motivated to do this because having the PLL's provide the synchronization capabilities would save on synchronization information that would have to be sent in the packets otherwise.

4. Regarding claim 35 more specifically, the combination of Smith and Laor et al. does not expressly disclose using both a clock recovered bus and a clocked bus. However, it would have been obvious to one of ordinary skill in the art to use both of these types of buses in the same system. One would have been motivated to do this because the one type of bus could act as a backup for the other bus in case of a failure, thus providing an additional redundancy in case of system failure.

5. Regarding claims 2, 3, 9, 10, and 17, as mentioned previously, the data inputs can support all sorts of data rates, from CBR to ABR to VBR (data bus has a first bus rate); this also means that the buses can support at least one bus rate. It also means that more than one of the ports can handle data of a first rate. Furthermore, it also means that two different sets of ports could handle two different rates of data.

6. Regarding claims 7 and 8, as shown in Figs. 2 and 13, any interface card can communicate with any other interface card through the switching units. Smith discloses that the system is bi-directional. See at least col. 8, lines 48-50.

7. Regarding claim 18, Smith nor Laor et al. expressly discloses grouping a first set of ports together into one telecommunication plane while grouping a second set of interfaces together into a second data plane, but it would have been obvious to a person of ordinary skill in the art at the time of the invention to group certain interfaces in this fashion. One would have been motivated to do this because keeping the phone communications and the data communications separate would allow for a more efficient system. By grouping similar types of data together, the system can take advantage of the redundancy to make for more efficient or faster transport.

8. Regarding claims 4 and 22, Smith discloses that for n inputs, the cell-routing process will take n+1 clock cycles (parallel data buses further includes a closed parallel data bus). See col. 21, lines 10-15. To provide these clock cycles, the system must contain a reference clock.

9. Regarding claims 11, 13, and 15, neither Smith nor Laor et al. expressly discloses the exact rate at which the data bus transmits data, but it would have been obvious to choose a value like 311 MHz. Likewise, the same reasoning applies to the STS-192 rate and the STS-48 rate for the lower speed. One would have been motivated to do this because those are standard rates found in the industry, so choosing those rates would make the product more commercially viable.

10. Regarding claim 16, Smith does not expressly discloses splitting one of the data streams into 4 and to transmit them over parallel buses to form a 32-bit stream. However, it is well-known in the art to split from serial to parallel in order to speed up data delivery. It would have

been obvious then to split the data stream in the combined system of Smith and Laor et al. into 4 different streams. One would have been motivated to do this because it would increase the rate of delivery, thus making the system more efficient in certain situations.

11. Regarding claim 36, neither Smith or Laor et al. expressly discloses sending the information that requires clock information over the clocked interface card or sending the information that didn't need a clock over the clock recoverable interface cards, but it would have been obvious to send the information that required a clock (i.e. synchronous information) with the clocked interface cards, and it would have been obvious to send the information that didn't need a clock (i.e. asynchronous information) with the clock recoverable interface cards. One would have been motivated to do this because it would be more efficient to use the clock recoverable interface cards for information that required clock information—sending information that didn't need the clock over the lines that are clocked would be a waste of resources.

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al, in view of Demiray et al. (US 5,740,157), further in view of Czerwiec et al. (US 5,161,152), and in light of the rejection to claim 1. Neither Smith nor Laor et al. expressly discloses a redundant controller nor a redundant cross connect unit. Demiray et al. discloses a redundant crossconnect unit for when outages occur in the line of the modules. See Abstract, and Fig. 1. Czeriec et al. discloses using redundant controllers. See col. 5, lines 22-26. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use redundant components in the system disclosed by Smith. One would have been motivated to do this because having redundant components can keep the system working in case of a failure to one of the components.

13. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al., further in view of Lamarche et al. (US 6,414,953), and in light of the rejection of claim 1. Neither Smith nor Laor et al. expressly discloses transmitting different protocols or using a housing. Lamarche et al. discloses a multi-protocol cross connect switch that can connect different protocols. See Fig. 1, and col. 2, lines 46-61. Lamarche et al. also discloses putting all of the interconnections in a housing. See Fig. 2, and col. 2, line 62-col. 3, line 17. It would have been obvious to use connect multi-protocols together and to use a housing to place all of the ports or cards. One would have been motivated to connect multi-protocols together because it gives the switch more functionality, and one would have been motivated to use a housing because that organizes the cards in an efficient manner.

14. Claims 12, 14, 20, 21, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al., further in view of Tarridec et al. (US 4,751,699), and in light of the rejection to claim 1. Neither Smith nor Laor et al. expressly discloses a 32-bit clock recovered bus or using an oscillator that is phase locked. Tarridec et al. discloses using 32-bit messages in a system that includes clock recovery using a phase locked loop and an oscillator. See at least col. 8, lines 33-58. It would have been obvious to use a 32-bit clock recovered parallel data bus with the oscillator operating at frequencies such as 155 MHz and 19 MHz as taught by Tarridec et al. in the combined system of Laor et al./Smith. One would have been motivated to do this because the PLL and the oscillator are useful components to use when it comes to clock recovery, where 155 MHz and 19 MHz are common frequencies used in industry.

15. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al. and further in view of Upp et al. (US 5,967,405), in light of the rejection to claim 1. Smith does not expressly disclose converting different formatted packets into a single format. Upp et al. discloses a variety of modules used with the ultimate result being a SONET formatted signal. See col. 2, lines 55-61. It would have been obvious to use a standard data format for all signals. One would have been motivated to do this because using a standard format in the crossconnect makes transmitting signals through it a simpler process.

16. Claims 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al., further in view of Kosugi et al. (US 5,189,410), and in light of the rejection to claim 1.

17. Regarding claim 25, Smith discloses multiple interface cards, where more than one stream of data can travel among the various combinations of input and output interface cards. Neither Smith nor Laor et al. expressly discloses additional data streams that include synchronization information. Kosugi et al. discloses having a first interface means for inserting frame synchronizing information. See col. 3, lines 30-55. It would have been obvious to insert such information into a frame. One would have been motivated to do this because having his information in frames would be more efficient in some cases than sending separate synchronization packets, which would need their own headers.

18. Regarding claims 26, 27, and 28, as mentioned previously, the system of Smith/Laor et al. can handle data of different rates, whether it be a second, third, or fourth rate.

19. Regarding claims 29, 30, 31, 32, 33, and 34, as mentioned previously, the STS rates can be chosen arbitrarily to meet industry standards, and the oscillator speed can be chosen so that the line will be properly clock recovered.

20. Claims 37, 40-44, 45, 47, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Laor et al., further in view of Madonna (US 5,737,320), and in light of the rejection to claim 1.

21. Regarding claims 37 and 45, neither Smith nor Laor et al. expressly discloses removing the first telecommunications signal from the first payload and inserting the first telecommunications signal in a second payload. Madonna discloses sending "empty" and "full" packets around a ring structure. For example, the first node in Madonna could send a "full" packet. The next node could remove the information that it needs from that packet. Later, another node could send out an "empty" packet and the node that removed that information initially could place that information back into the "empty" packet for transmission to another node. See at least col. 14, line 13-col. 15, line 17. It would have been obvious use the teachings of Madonna that concern the unloading and loading into the different payloads in the system disclosed by the combination of Smith and Laor et al.. One would have been motivated to do this because the crossconnect unit may want to examine the payload data (i.e. check for errors), before sending it further along the network.

22. Regarding claims 40, 41, 47, and 48, neither the combination of Smith/Laor et al. nor Madonna expressly discloses pre-aligning the signal by a certain offset, but it would have been obvious to pre-align the signal by a certain offset. One would have been motivated to do this because if the signal is pre-aligned, it would be easier to send the signal. That is, it won't be

necessary to perform certain steps to make sure the payload and the signal are aligned because the two will have been pre-aligned with the offset, and the signal can be transferred faster.

23. Regarding claim 42, as mentioned previously, Smith discloses multiplexing signals together for form an "aggregate".

24. Regarding claims 43 and 44, "removing the aggregated signal from the 3rd payload" and inserting this into the 4th payload is the same concept as removing from a first payload and inserting into a second payload. This concept has already been discussed with regard to the rejection of claim 37.

25. Claims 38, 39, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Madonna in further view of Lamarche et al. See the previous rejection that involved Lamarche et al. Neither the combination of Smith/Laor et al. nor Madonna expressly discloses transmitting different protocols or using a housing. Lamarche et al. discloses a multi-protocol cross connect switch that can connect different protocols. See Fig. 1, and col. 2, lines 46-61. Lamarche et al. also discloses putting all of the interconnections in a housing. See Fig. 2, and col. 2, line 62-col. 3, line 17. It would have been obvious to use connect multi-protocols together and to use a housing to place all of the ports or cards. One would have been motivated to connect multi-protocols together because it gives the switch more functionality, and one would have been motivated to use a housing because that organizes the cards in an efficient manner.

Response to Arguments

26. Applicant's arguments filed February 2, 2004 have been fully considered but they are not persuasive.

27. In response to Applicant's argument that the combination of Laor et al. and Smith does not disclose a clock recovered bus, the Examiner respectfully disagrees. One of the purposes of a PLL is to perform clock recovery on a line. As described in Applicant's specification on pages 14-16, clock recovery for the bus is performed by the interface and cross-connect cards. This clock recovery is accomplished through the use of a reference oscillator. A loop filter and a reference clock are also used. See page 14, line 26-page 15, line 26. Thus, the clock recovery in Applicant's invention essentially uses all of the elements used in the phase locked loop system described in Laor et al.. The system of Laor et al. uses a frequency source, or an oscillator, and a clock to help the lines and system become clock recovered. Because Applicant's specification describes the same functionalities as described in Laor et al., Laor et al. discloses the use of clock recoverable lines.

28. In response to Applicant's argument that the combination of Laor et al. and Smith does not disclose <u>not</u> sending synchronization information, the Examiner respectfully disagrees. The advantage of using a PLL is that it employs a feedback loop. Using this feedback loop, the PLL is able to become synced with no need for synchronization information to be passed anywhere. The reason that Laor et al. does not include the negative limitation is because it would be well-known to someone in the art that the PLL in this system takes care of the syncing by itself. Because the sending synchronization information would be superfluous in a system like Laor et

al., Laor et al. inherently discloses that synchronization information will not be included in a data stream.

29. In response to Applicant's argument there is no suggestion of grouping interfaces in the combination of Smith and Laor et al, the Examiner respectfully disagrees. It would have been obvious send similar types of data together over certain interface cards. The motivation is explained now in the rejection.

30. In response to Applicant's argument that there is no suggestion in the combination of Smith and Laor et al. that any first card can communicate with any second card, the Examiner respectfully disagrees. As is more clearly stated in the rejection, Smith discloses that interfaces can be bi-directional, meaning that ports can handle inputs and outputs. Thus, it follows that any card can receive from any other card.

31. In response to Applicant's argument that the combination of Smith, Laor et al., and Madonna does not disclose extracting information from a first packet at a first node and sending that information to a second node using a second packet, the Examiner respectfully disagrees. While it may be true the information in the first packet may be first destined for the first node, it is possible that this information can be processed by the first node before being sent onward to a second node. Claim 37 only mentions that transmitting in the second payload must include "at least" the first telecommunications signal. This leaves open the possibility that other information along with the information found in the first packet can be put into the payload of this second packet. A signal can certainly be destined for more than one destination, so it could travel to both a first and a second node, but this doesn't have to occur at the same instant. Because this

possibility exists, the combination of Smith, Laor et al., and Madonna discloses the aforementioned claim limitation.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy Lee whose telephone number is (703)305-7349. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703)305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLL
Timothy Lee
May 13, 2004

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